Application Note

AN2467/D
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Power Quad Flat Pack No-Lead (PQFN)

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1.0 Purpose

This document provides guidelines for Printed Circuit Board (PCB) design and assembly. Package performance attributes such as Moisture Sensitivity Level (MSL) rating, board level reliability and thermal resistance data are included as reference.

2.0 Scope

This document is written to generically encompass several different Power Quad Flat No-lead (PQFN) packages assembled at Motorola internal assembly sites and external subcontractor sites. It should be noted that device specific information is not provided. This document serves only as a guideline to help develop a user specific solution. Development effort will still be required by end users to optimize PCB mounting processes and board design in order to meet individual-specific requirements.

3.0 Power Quad Flat No-lead (PQFN) Package

3.1 Package Description

The PQFN is a surface mount plastic package with lead pads located on the bottom surface of the package. All PQFN packages have either been designed with a single exposed die pad (flag) or multiple exposed die pads depending on device requirements and intended application. The industry standardization committee, JEDEC, will have design guidelines and structure descriptions for these package types when established. This JEDEC registration is in-progress for several PQFN designs.

3.1.1 Package Application

The PQFN surface mount packages have been designed to meet the high power dissipation requirements of automotive, industrial, and commercial applications. Features such as solder die attach material, thick copper lead frames, exposed heat sinks, and heavy gauge aluminum wire capability allows for efficient heat transfer out of the PQFN packages.

3.1.2 Package Dimensioning

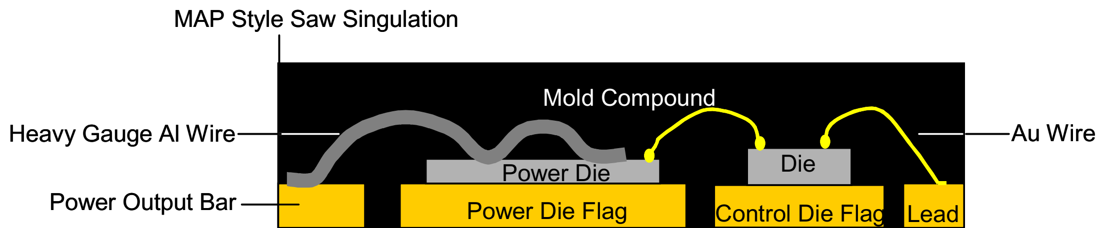
Currently, there are PQFN packages ranging from 10 x 10 mm to 12 x 12 mm in body size. Lead counts range from 16 to 35 at this time. The lead pads have been designed in both single-row and double-row configurations depending upon the specific package requirements. The lead pitch of the perimeter leads is either 0.8 or 0.9 mm.

3.1.3 PQFN Package Design

While there are many different package configurations available, the PQFN package platform differs from the standard QFN package platform (JEDEC: M0-220) by having the following characteristics in Table 1.

Table 1. Differences Between QFN and PQFN Packages

Characteristic	QFN (JEDEC: MO-220)	PQFN
Lead Pitch	0.65 mm or less	0.8 mm or more
Leadframe Thickness	0.13 - 0.20mm (5 - 8 mil) Cu	0.51mm (20 mil) Cu
Package Thickness	1.0mm or less	2.1 mm
Die Attach	Epoxy Only	Epoxy and/or Solder
Wire Bonding	(1.0 mil – 2.0 mil) Au Wire	Small gauge Au and large gauge Al
Exposed Flags	1 Flag	1 or more flags



Singulation is similar to that of the original QFN package.

Figure 1. Cross-Section of a Custom PQFN MAP (Molded Array Package)

3.2 PQFN Assembly Process Flow

Figure 2 displays the PQFN assembly process flow steps referred to as Mold Array Packaging (MAP). The MAP process steps are very similar to the QFN process steps except for the addition of solder paste die attach, de-flux with de-ionized water rinse and taping process steps. The wire bond process may include both Au wire ball-bonding as well as Al wire wedge-bonding, depending on the application requirements. The molded array is singulated with a saw scribing process that leaves vertical edges on the body of the PQFN packages.

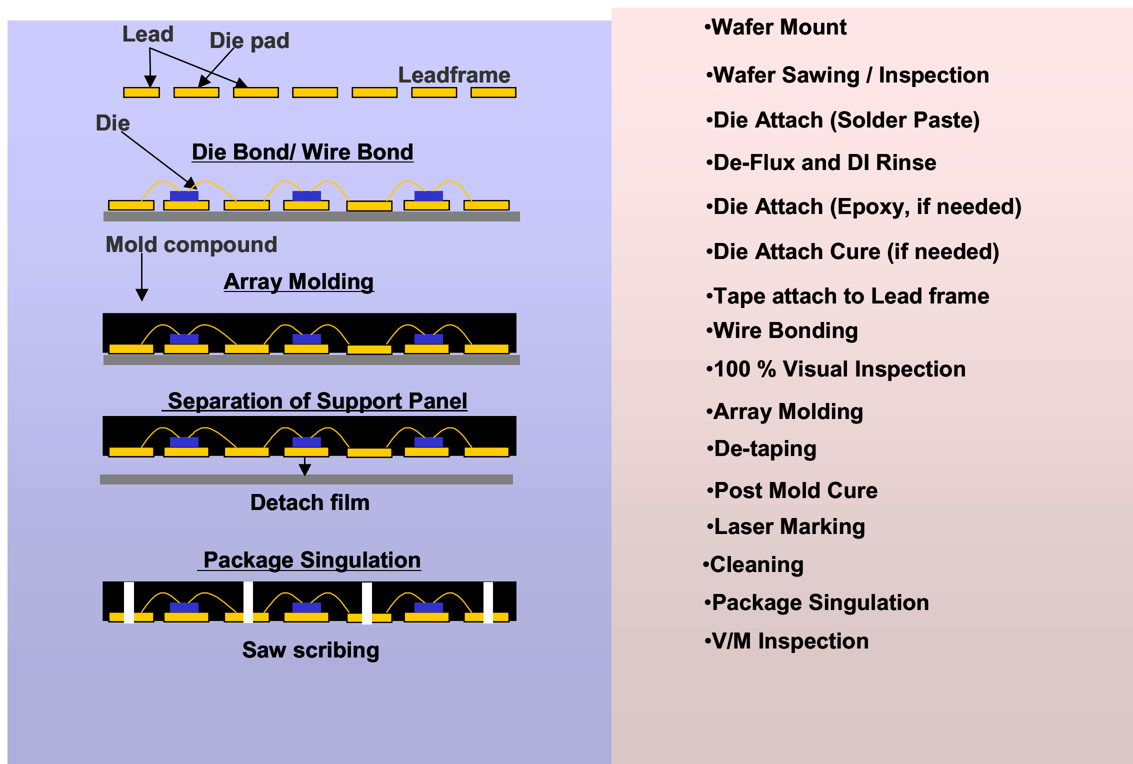


Figure 2. Mold Array Packaging Process Flow for the PQFN Package

4.0 Printed Circuit Board Guidelines

4.1 Printed Circuit Board Design for PQFN Packages

PQFN packages have unique and varied footprints due to the use of exposed pads for thermal management. Care should be taken to design pads on a PCB that are compatible with the arrangement of unique features on the bottom side of PQFN packages. The following guidelines can be used to help address a user specific solution.

The board design should begin with copper pads that sit beneath the periphery leads of a mounted PQFN. These board pads should extend outside the PQFN edge a distance of approximately 0.15mm. See Figure 3. The extra solder that will form outside the package edge will create a useful, yet imperfect, visual indication of solder joining the package after reflow processing, as shown in Figure 4. The copper board pads should also extend beneath the package approximately 0.10mm beyond the inner lead edge, as shown in Figure 3.

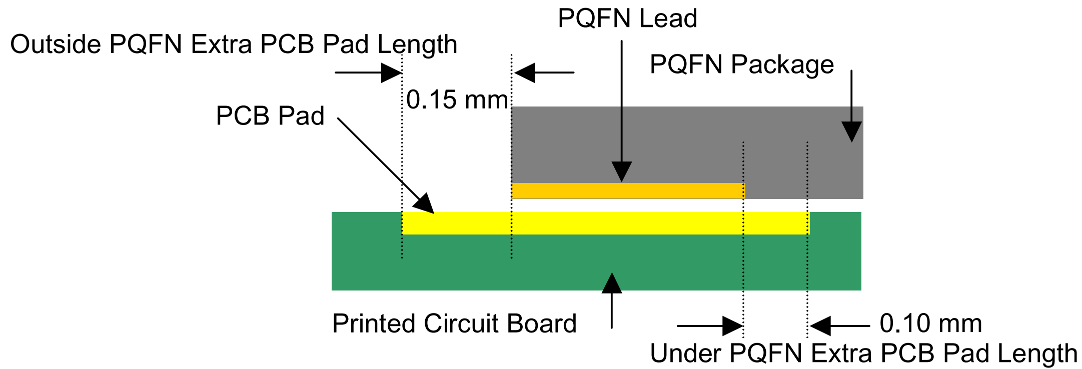


Figure 3. A Cross-Section of Package Lead and Suggested PCB Pad

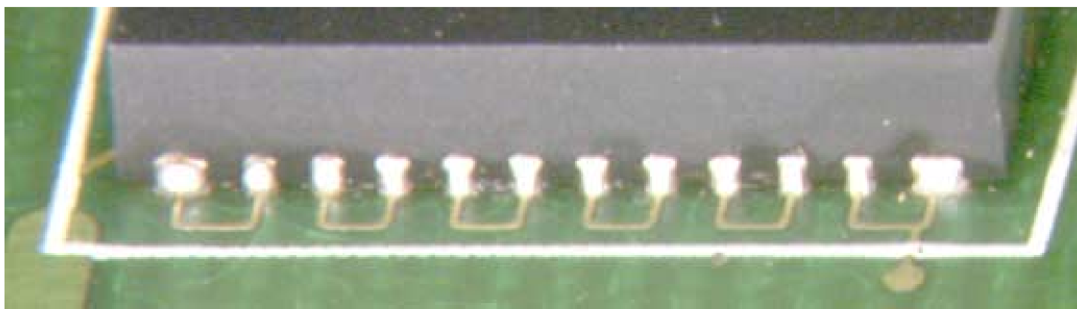


Figure 4. Example of Visible Solder-Joint Exterior to a PQFN Package

The pad width should be approximately 0.025mm wider than the nominal lead dimension on each side. See Figure 5. Increasing the pad width 0.025mm on both sides (0.05mm total) helps with placement of parts during assembly by allowing a larger target for the PQFN to be seated. It will be important to keep at least 0.15mm board spacing between adjacent pads. The 0.15mm spacing will keep solder from bridging between neighboring leads, thereby electrically shorting them together.

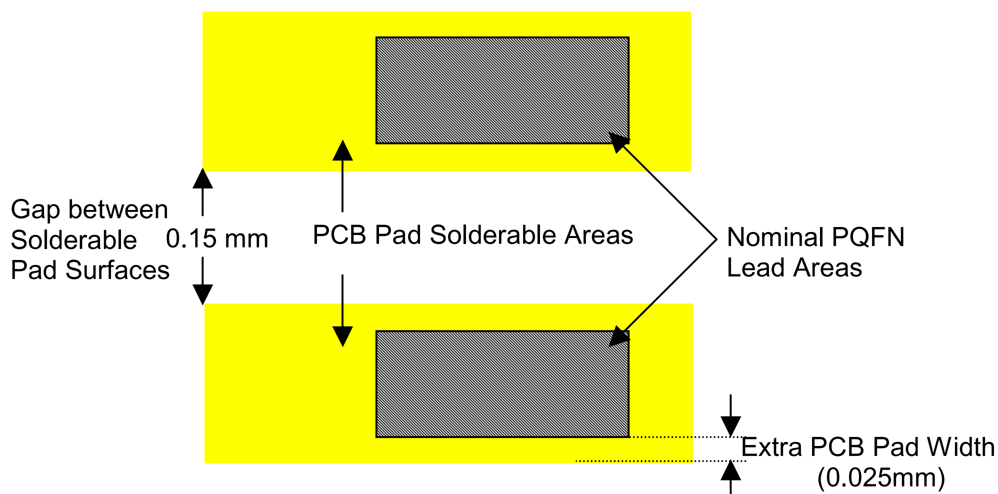


Figure 5. Top View of PCB and Suggested PCB Pad Size for PQFN Leads

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After completion of the periphery pad design, the larger exposed pads will be designed to create the mounting surface of the PQFN exposed heat sink(s). The primary transfer of heat out of the PQFN will be directly out the bottom surface of the exposed heat sink(s). It is recommended to use an array of plated through-hole vias beneath the mounted part to aid in the transfer of generated heat into the PCB. The specific diameter and pitch of the via hole array will need to be defined by the end user are typically consistent in size with other drill hole diameters found on the application PCB. The JEDEC committee proposes an array of plated vias for thermally standardized testing with via hole diameters of 0.3mm with a center-to-center pitch of 1.2mm per JESD51-5. This via pattern can be used as a starting point for creating a customer specific board design.

A PCB exposed pad that is lined with periphery pads, having at least 0.15 mm spacing between the pad edge and the exposed pad, would again provide some assurance against solder bridging. Since there can be a large volume of solder needed beneath the package, to cover the large exposed pad region, the 0.15mm spacing can be increased to approximately 0.25mm. See Figure 6. There will often be a resulting PCB exposed pad that is smaller in size than the PQFN exposed heat sink(s) after the application of the noted guidelines. See Figure 6. It is okay if this situation exists since there will likely be a sufficient volume of solder beneath the PQFN exposed heat sink to mount the package.

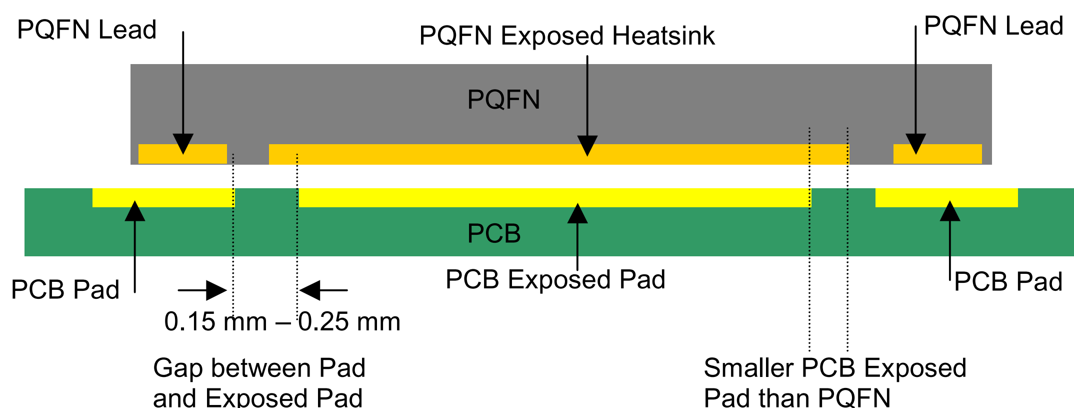

Figure 6. Example of Spacing Between PCB Pad and Exposed Pad

4.2 Solder Paste Stencil Design for PQFN Packages

In general, solder paste stencil aperture openings can be on-to-one (1:1) with the peripheral PCB pad sizes. However, the stencil aperture openings should be smaller than the large PCB exposed pad regions to reduce the chance of solder bridging. There will be a larger volume of solder in the PCB exposed pad region so it is necessary to create additional physical space between the exposed pad and the surrounding PCB pads. It is suggested to reduce the stencil aperture opening by a minimum of 0.25mm as seen in Figure 7.

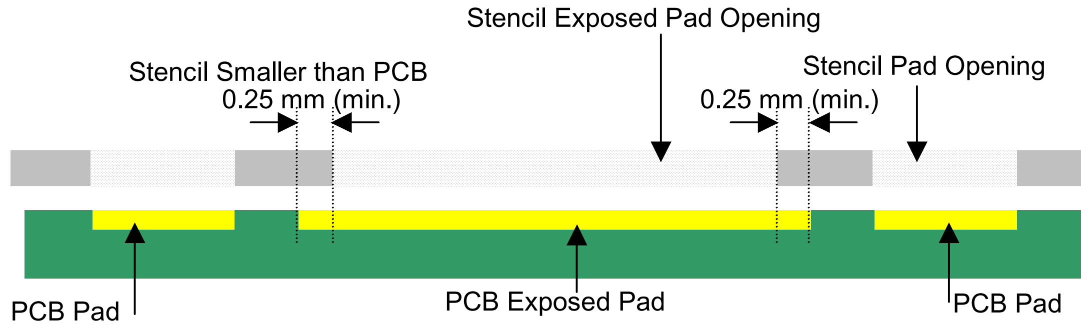

Figure 7. Reduced Solder Stencil Aperture for Exterior of Exposed Pad

During the solder screen print operation, a stencil blade can both deposit solder paste and remove, or "scoop" it in large aperture openings. In the large openings, the blade bends down into the opening thereby leaving less solder volume than anticipated. To mitigate the effect of scooping, the aperture can be broken up into an array of smaller openings. The array of openings will resemble a "window pane" pattern as seen in Figure 8. Large PCB exposed pads that are approximately 3.2mm x 3.2mm or larger in size should have a "window pane" stencil opening pattern. It is suggested that a spacing of 0.25mm is used between the individual panes. See Figure 8. This recommendation must be confirmed by solder reflow processing followed by X-ray analysis. Any voiding in the reflowed solder should be minimized. It is possible to get incomplete wetting between the PQFN and the PCB exposed pad. Incomplete wetting can occur if the "window pane" pattern is not properly optimized with the reflow wetting process.

Stencil thickness can play an important role in solder joining. The stencil thickness is usually chosen by a combination of both typical industry practices and the requirements of the other components on a PCB module. Motorola has had success with solder joining processing by using stencil thickness of both 0.125mm and 0.150mm (5 and 6 mils). If stencils with a thickness greater than 0.150mm are used, it is suggested to investigate a reduction of the stencil opening size, thereby reducing total solder volume to minimize the risk of solder bridging. For stencils thinner than 0.125mm, aperture openings may have to be increased in order to provide enough volume of solder to get complete solder wetting between all contact surfaces.

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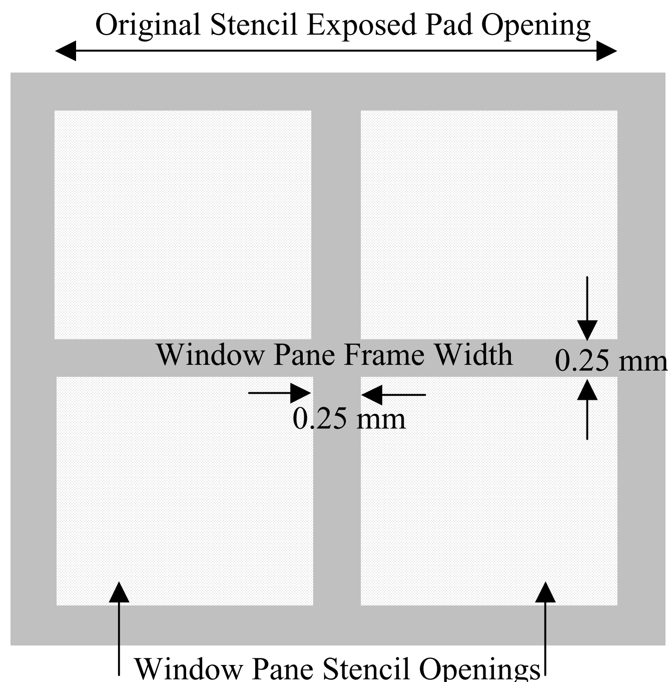

Figure 8. Window Pane Pattern for Exposed Pad Stencil Opening

5.0 2nd Level Reliability Data: Experimental Solder Joint Analysis

Several 16 PQFN packages (Fig 8.1) were mounted using a eutectic ($Sn_{37}Pb_{63}$) solder, to a 2-layer PCB that is considered typical of many automotive and industrial application designs. The PCB had a total thickness of 0.65mm with 70um thick copper layer on both top and bottom surfaces. Half of the test boards were mounted to thick Aluminum plates with an industry common adhesive tape. The attached plates simulated the mechanical forces found in typical automotive electronic modules that are mounted within an aluminum housing. The test boards with mounted PQFN packages were placed into temperature chambers for cycling. A package "failure" was recorded when any single solder joint failure occurred. The data in Figure 9 was generated by air-to-air thermal shock (AATS) cycling between –40ºC and 125ºC. One cycle consisted of 15 minutes at each temperature extreme and a very short transfer time between chambers. Air-to-air thermal shock is an accelerated solder joint reliability test that Motorola uses to quickly determine reliability in an application design. Gathered AATS data is to be compared with air-to-air temperature cycling (AATC) data to find correlation that will allow predictive analysis of reliability in a shorter time period. The Weibull plots shown in Figure 9 and Figure 10 can be used to determine the predicted first time to failure (FTTF) based upon a correlation plot of measured failures. The predicted FTTF is estimated to be the number of cycles measured when the linear correlation line crosses the horizontal axis.

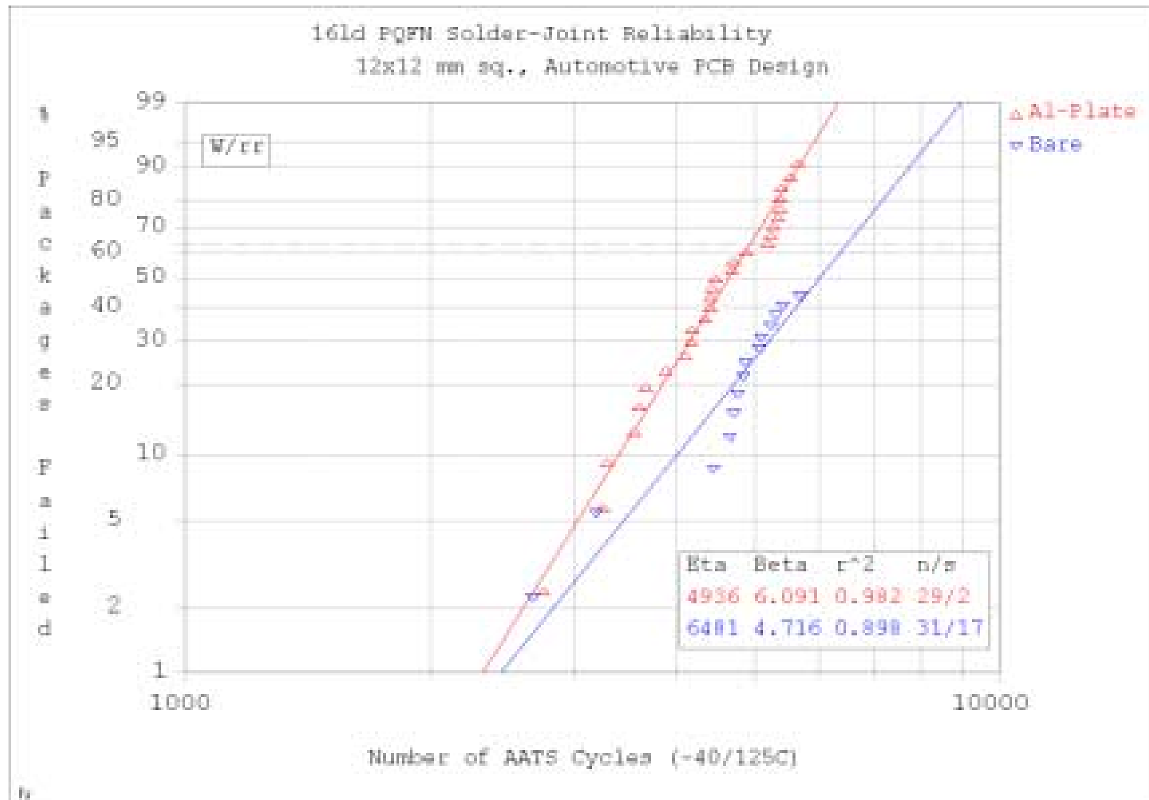

Figure 9. Solder-Joint Reliability for Air-to-Air Thermal Shock of 16 PQFN Packages

At the time of this writing, the AATC study had accumulated 3743 cycles of –40ºC and 125ºC cycling. The AATC study will remain in progress until 75% failure is achieved. One cycle of AATC consists of a 1-hour duration with a 15-minute dwell at temperature and 15-minute ramps between temperature extremes. The first recorded failure for the aluminum plated PCB boards occurred at 2308 cycles with 9 more failures to date. See Figure 10. The bare PCB board group, with less mechanically induced forces, had the first failure reported at 3280 cycles with 2 more additional failures to date. The results of the AATC reliability data are plotted in Figure 10. Motorola will complete this set of experiments and provide updates that can be obtained through Motorola sales offices and/or updates application notes. As more PQFN packages are designed, Motorola will continue to more gather solder joint reliability data as needed.

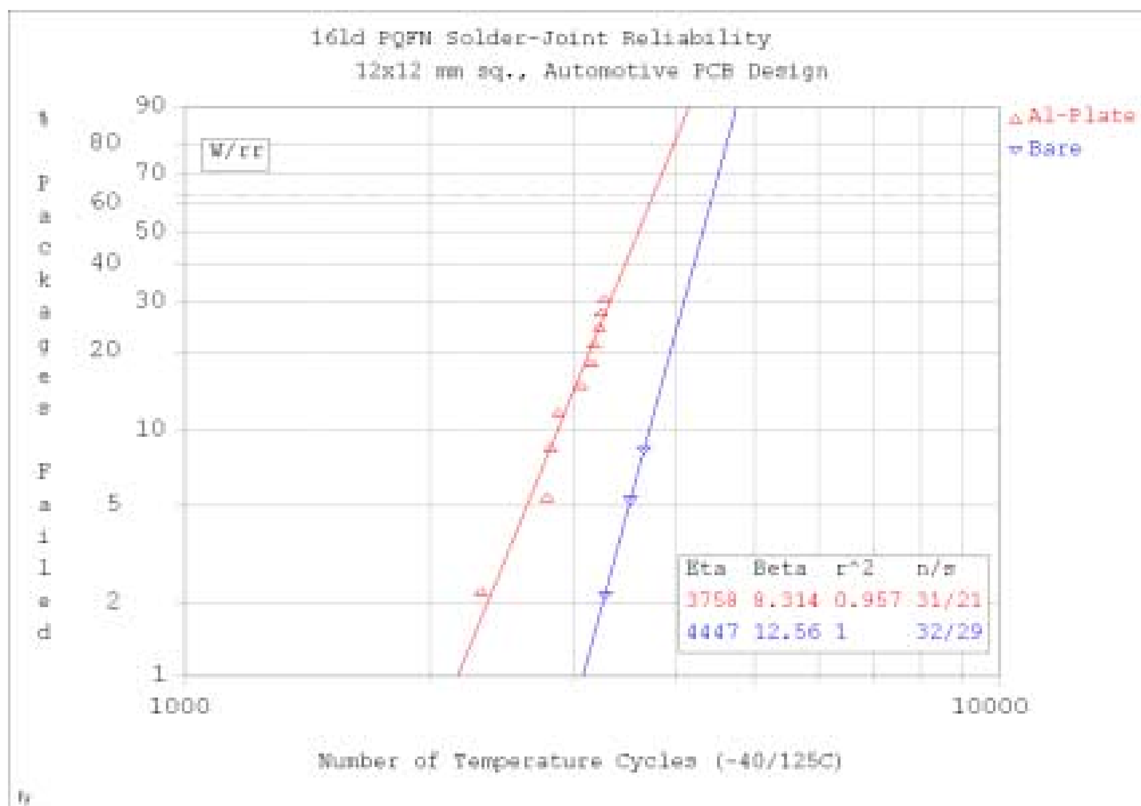

Figure 10. Solder Joint Reliability for Air-to-Air Temperature Cycling of 16 PQFN Packages

The solder joint reliability data in Figure 9 and Figure 10 should be considered achievable under similar mounting and testing conditions. Customer specific board designs and temperature cycling ranges will vary results. End users are encouraged to conduct their own solder joint reliability experiments.

6.0 Theoretical Solder-Joint Reliability Modeling Results

Motorola has conducted finite element model simulations of the creep and strain that PQFN solder-joints would experience during temperature cycling. Results indicate that the solder-joints with highest strain rates are those at the corner of the package. These solder joints have the most strain at the pad backside under the package and not at the fillet solder located on the exterior bottom edge of the packages. The large exposed pads of the PQFN see little to no strain during temperature cycling. Motorola will continue to refine the simulation as more experimental data becomes available and as more devices are packaged into PQFN type packages.

7.0 Thermal Performance Modeling Results

The 16 PQFN package has been modeled to obtain thermal performance values. Figure 11 shows a top-view of the single-layer printed circuit board measuring 80mm x 80mm x 1.6mm used in the thermal model. A 35um thick copper top-layer formed the lead traces and also a heat spreader area, represented by “A”. The heat spreader area was used to remove heat from the bottom surface of the PQFN and spread it onto the PCB. A copper strip that was 0.3mm in width was modeled directly beneath the PQFN and in contact with an exposed heat sink.

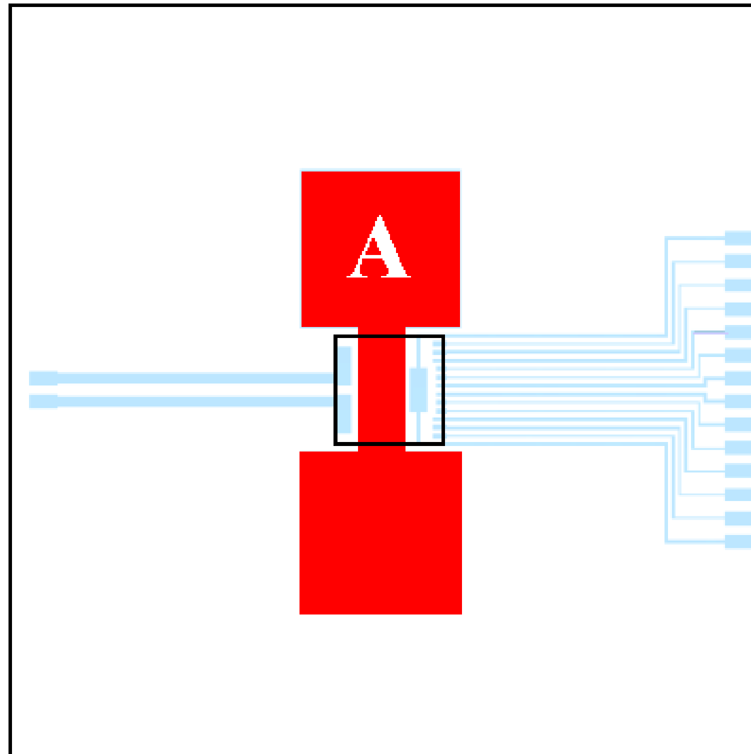

Figure 11. Thermal Model of a MC33982FC in a 16 PQFN Package Mounted to a Single-Layer PCB

The board used in the modeling produced conservative results considering it is a single-layer PCB that has a layer of copper on the top surface only. A more efficient board design would include a multi-layer board with plated through-hole vias beneath the mounted part. The heat could then transfer through the board and spread to the connected Cu layers or possibly to a larger heat sink such as a metal module housing. The model was performed with various sizes of heat spreader areas, labeled “A”, to represent the effect of improving dissipation onto the PCB. Table 2 is a summary of resulting thermal resistance values obtained for a range of convection coefficients (h). The convection coefficient will range from approximately 5W/mK to 10W/mK for natural convection (still air) applications in a broad array of mounting conditions. Mounting conditions could include vertical or horizontal mounting in open air or inside a closed container such as a module housing. The thermal resistances from the die junction to the ambient, case, and lead pad are reported.

Table 2. Steady State Analysis Summary of MC33982FC in a 16 PQFN Package

	A (mm)²	h (W/m²K) 7	8	9	10
RthJA	0	91	86.2	81.9	78.2
°C/W	300	74.3	69.4	65.4	62
	600	43	40.1	37.7	36
RthJC	0	0.9	0.8	0.9	0.8
°C/W	300	0.8	0.8	0.8	0.9
	600	0.5	0.6	0.6	0.9
RthJB	0	29.4	29.2	28.9	27.8
°C/W	300	22.4	22.1	21.8	21.1
	600	12.9	12.8	12.7	11.8

Note: RthJA = Thermal Resistance Junction-to-Ambient
RthJC = Thermal Resistance Junction-to-Case
RthJB = Thermal Resistance Junction-to-Lead

As the heat spreader area “A” is increased, the thermal resistance from junction to ambient will be reduced. This occurs because the junction temperature will be reduced when the generated heat can be transferred away from the package more effectively as seen in Figure 12. In an actual application, heat transfer can be improved through Cu heat spreader planes on both top and bottom surfaces to two-layer boards. Internal Cu planes can also be used to spread heat in multi-layer PCB applications.

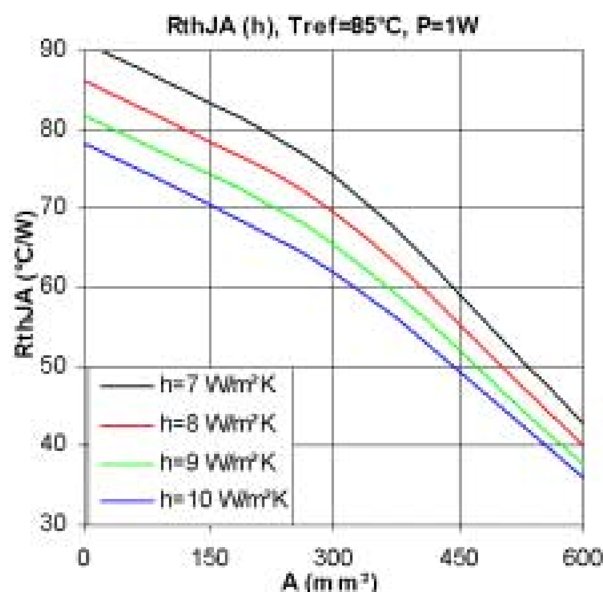

Figure 12. RthJA (Junction-to-Ambient) Resistance Versus Heat Spreader Area

In a steady state condition, Figure 12 shows that the heat spreader area can greatly affect the thermal resistance for the same mounting conditions. The benefit of thermal heat spreading in a PCB for transient conditions can also be seen in Figure 13. Figure 13 shows detail of the initial transient response curve for 1Watt

power dissipation at a relatively high convection coefficient condition (h=10W/m^{2}K). The transient thermal resistance is inversely related to the amount of heat spreader area is provided.

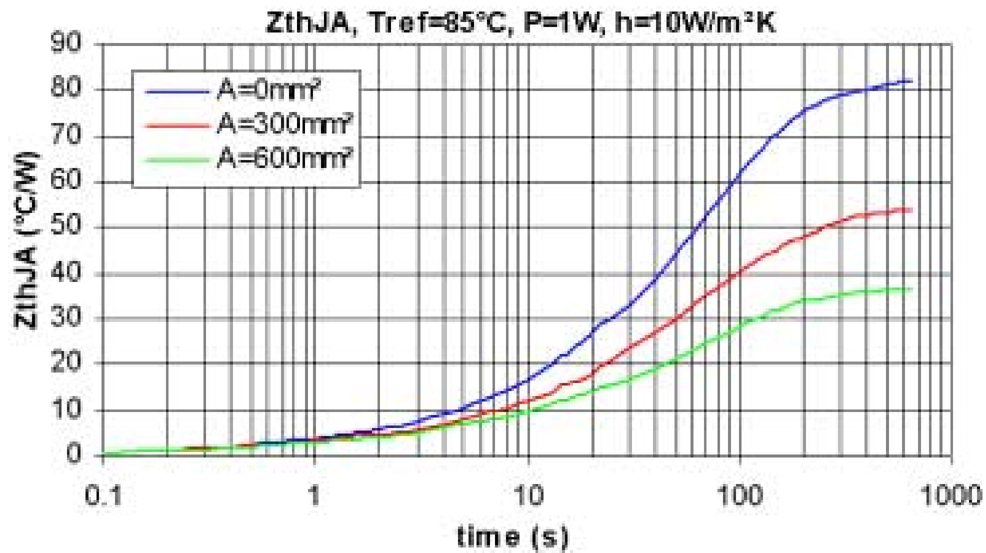

Figure 13. Transient Analysis of ZthJA for MC33982FC in a 16 PQFN Package

Figure 13 represents the full transient response of the junction-to-ambient thermal resistance, RthJA, until steady state response is reached near 600 seconds. The boundary conditions modeled between Figure 12 and Figure 13 remain the same for comparison.

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8.0 APPENDIX

8.1 Case Outline Drawings

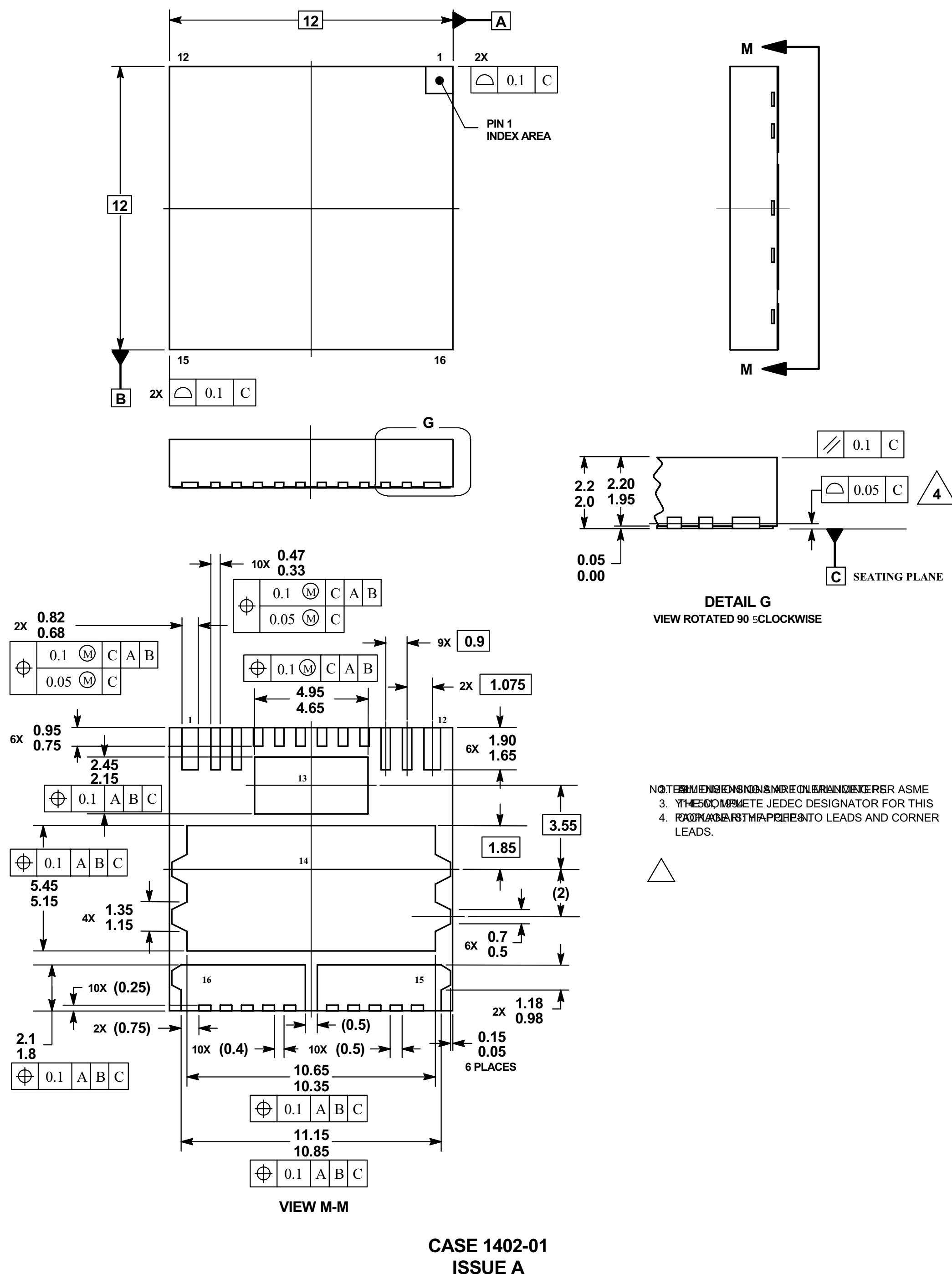

Figure A-1. 16 Lead PQFN, Case No. 1402

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CASE 1431-01
ISSUE O

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Figure A-2. 22 Lead PQFN, Case No. 1431

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10 A
10 1
2X 0.1 C
21 29
22 28
10
PIN 1 INDEX AREA
24 26 27
PIN NUMBER REFERENCE ONLY
B 2X 0.1 C

M
G
M

NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
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0.1 C
2.2 2.0
2.20 1.95
0.55 0.35
0.05 C 4
0.05 0.00
0.65 0.35
C SEATING PLANE
DETAIL G
ROTATED 90° CLOCKWISE

7.65 7.35
0.1 A B C
PIN NUMBER REFERENCE ONLY
VIEW A
1 2 5 6 7 10
11 12 15 16 17 20
0.1 A B C
29 21
28 22
23
2.4 2.1
1.375
25
2X 4.9 4.6
0.1 A B C
VIEW B
27 26 24
9X (0.25)
2X (0.5)
2.15 1.85
0.1 A B C
2X 3.65 3.35
0.1 A B C
VIEW M-M

8X 0.47 0.33
0.1 Ⓜ C A B
0.05 Ⓜ C
2X 0.62 0.48
0.1 Ⓜ C A B
0.05 Ⓜ C
6X 0.8
2X 0.875
5X 0.90 0.65
5X 0.90 0.65
2X 0.47 0.33
0.1 Ⓜ C A B
0.05 Ⓜ C
0.8
1.45
2X 0.90 0.65
VIEW A

0.1 Ⓜ C A B
1.65 1.35
1
3.625
2.9 2.6
0.1 Ⓜ C A B
8X (0.4)
(1.5)
2X (0.55)
8X (0.4)
0.1 Ⓜ C A B
2.15 1.85
VIEW B

CASE 1445-01
ISSUE O

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Figure A-3. 29 Lead PQFN, Case No. 1445

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12 A
14 1 2X
15 35 0.1 C
PIN 1 INDEX AREA
12
22 28
24 27
B 2X 0.1 C
PIN NUMBER REFERENCE ONLY
M
M

G

0.1 C
2.2 2.0
2.20 1.95
0.05 C 4
0.05 0.00
C SEATING PLANE
DETAIL G

0.1 M C A B
30X 0.62 0.48
8.84 8.54
0.1 M C A B
0.05 M C
13X 0.8
2X 1.25 1.00
0.4
28X 0.90 0.65
7X 0.8 2 PLACES
1 14 35 15
0.44
8.77 8.47
0.1 A B C
2.31
28 22
2.15 1.85 0.1 A B C
23
4X 1.50 1.25
(0.25)
27 26 25 24
(0.25)
2X 1.67 1.53
2X 4.15
0.1 M C A B
0.05 M C
2X 2.87 2.73
0.1 M C A B
0.05 M C
11.15 10.85
0.1 A B C
VIEW M-M

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Figure A-4. 35 Lead PQFN, Case No. 1438

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